

## AMENDMENT

The Commissioner is hereby authorized to charge payment of any additional fees involved with added Claims and the like to Deposit Account No. 19-0033.

## IN THE CLAIMS

Please amend claim 29, 33-35 as follows:

29. (AMENDED) A stacked-gate flash memory having a shallow trench isolation with a high-step oxide and high lateral coupling comprising:
- 1 a substrate having a gate oxide layer;
  - 2
  - 3
  - 4
  - 5
  - 6 at least two trenches formed to a depth between about 2500
  - 7 to 5000 Å below the surface of said substrate;
  - 8
  - 9 an oxide layer formed over said substrate, including over
  - 10 the inside walls of said two trenches;
  - 11
  - 12 a high-step oxide formed within said two trenches over said

oxide layer and protruding upward over the surface of said  
15 substrate to a height between about 2000 to 6000 Å;

said high-step oxide forming an opening with high walls  
18 over the surface of said substrate between said two  
trenches;

21 a first conductive layer formed conformally inside said  
opening and over the surface of the substrate between said  
high walls to form a floating gate having folding surfaces;

24 an intergate oxide layer formed over said floating gate  
having folding surfaces;

27 a second conductive layer formed protruding downward in  
between said folding surfaces over said intergate oxide  
30 layer to form a control gate; and

a self-aligned source (SAS) line.

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33. (AMENDED) The stacked-gate flash memory cell of claim  
29, wherein said opening has a width between about 1500 to  
3 5000 Å.

- 34*  
*cont*
- 34.** (AMENDED) The stacked-gate flash memory cell of claim 29, wherein said first conductive layer is polysilicon  
3 having a thickness between about 100 to 500 Å.

- 35.** (AMENDED) The stacked-gate flash memory cell of claim 29, wherein said second conductive layer is polysilicon  
3 having a thickness between about 1000 to 3000.